What is claimed is:

1. A single bit FIR filter comprising:

an input adapted to receive a plurality of serial input bits, said input bits being a single bit wide; said input comprising a predetermined number of input nodes; said input nodes separated into one or more sets of input nodes; said input adapted to allow said plurality of input bits to shift down the length of said input;

a storage device having a plurality of memory locations, each said memory location having an address such that bits in a first set of input nodes can be utilized to address one of said memory locations;

an output providing an accumulation of the contents of said the memory locations that were addressed.

2. The single bit FIR filter of claim 1, wherein said input has a single set of input nodes.

3. The single bit FIR filter of claim 1, wherein said input further comprises a second set of input nodes such that bits in said second set of input nodes can be utilized to address a second one of said memory locations, said output providing an accumulation of the contents of first and said second memory locations.

4. The single bit FIR filter of claim 1 further comprising an accumulator for receiving the contents of said addressed memory locations such that the output of said single bit FIR filter is an accumulation of the contents of said addressed memory locations.

5. A single bit FIR filter for comprising:

an input portion for receiving a stream of serial input bits, said input portion comprising a plurality of input node sets, each said input node set is for receiving input bits from said serial stream of input bits;

a memory comprising memory locations having an address and a value, said memory locations adapted to be addressed indirectly or directly by the contents at least one of said input node sets

an accumulator adapted to receive the contents of said addressed memory locations; said accumulator adding said contents of said addressed memory locations and producing a result; said result being substantially an output of said single bit FIR filter.

6. The single bit FIR filter of claim 5, wherein said memory locations are addressed indirectly by having said contents of a first input node set be subjected to an address offset prior to being provided to said memory.

7. The single bit FIR filter of claim 5, wherein each input node set comprises the same number of input nodes.

8. The single bit FIR filter of claim 5, wherein said input node sets comprise shift registers.

9. A method for providing a single bit FIR filter comprising:

receiving serial data into an input, said input being divided into sets of input data;

using each set of input data to directly or indirectly address memory locations associated with each set of input data;

reading the contents of said addressed memory locations;

accumulating the contents of said addressed memory locations

providing a single bit FIR filter output.

10. The method of claim 9 further comprising, after said using step, shifting said input data at least one input data position.

11. The method of claim 9 further comprising shifting said input data at least one input data position and after said step of providing repeating said method starting at said step of receiving.

12. The method of claim 9 further comprising loading said memory locations with values prior to the step of receiving.

13. The method of claim 9, wherein each set of input data comprises the same number of input bits.

14. A method of providing a single bit FIR filter comprising:

inputting a first bit of a serial stream of data into an input portion;

dividing said input portion into sets of data that can be used to address a memory directly or indirectly;

addressing a memory location of said memory with at least one set of data;

reading the contents of said memory location;

accumulating the contents of said memory location with the contents of other memory locations; and

providing an output of said accumulator as an output.

15. The method of claim 14, wherein each said set of data can be adapted to be used as an address.

16 The method of claim 14, wherein a set of data can be used to address a memory indirectly by providing said set of data with an offset.

17. The method of claim 14 wherein said input portion is at least on of 8, 16, 32, 64, or 128 bits long.